In the Specification:

Please replace the paragraph beginning on page 10, line 3, with the following rewritten paragraph:

Figure 5 illustrates a memory subsystem 500 according to another embodiment of the present invention. The memory subsystem 500 has a distributed memory controller arrangement similar to that illustrated in Figure 4 represented by registers 504 and 554. Each of the registers 504 and 554 are located in a respective memory controller. The ~~memory subsystem 580~~ memory subsystem 500 further includes addressable memory areas represented by memory arrays 508 and 558. The memory array 508 is segmented into m memory blocks and the memory array 558 is segmented into n memory blocks. The register 504 includes start address field 512, memory size field 514, and memory valid field 516, and a number of BANK fields 518-526. Each of the BANK fields 518-526 corresponds to a memory block in the memory array 508. The register 554 includes start address field 562, memory size field 564, and memory valid field 566, and BANK registers 568-574. Each of the BANK fields 568-574 corresponds to a memory block in the memory array 558. The start address field 512 and memory size field 514 are programmed with the start address and memory size for the memory array 508. As explained previously, these values are referenced by the respective memory controllers in order to determine whether to pass a memory access request it receives to another memory controller in order to access the requested memory location.